Amorphous Indium Oxide FEFETs Enabling Ultra-low Write Voltage and >10^{12} Endurance, >6 days Retention at 85°C for High-Density, Refresh-free Embedded Memory

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Emerging data-intensive workloads in artificial intelligence, high-resolution imaging, and real-time analytics demand embedded memory solutions that combine ultrahigh density, rapid access, and minimal energy consumption [1]. Conventional static RAM (SRAM) cells face fundamental scaling limitations due to their large footprint and volatile nature, while alternative technologies such as eDRAM and MRAM suffer from periodic refresh penalties or elevated write energy [1]. Ferroelectric field-effect transistors (FEFETs) based on HfO_2 gate dielectrics and conventional Si channel offer the potential for refresh-free, nonvolatile operation, but typical implementations require write voltages of ±4 V and exhibit endurance below 10^{10} cycles [2]. This work demonstrates the first back-end-of-line (BEOL)-compatible W-doped indium oxide (IWO) channel FEFET with sub-1V logic-compatible operation, enabling monolithic three-dimensional integration on FEOL at temperatures ≤ 400 °C. The device architecture in this work comprises a 4.5 nm amorphous IWO channel and a 5 nm HZO ferroelectric gate stack deposited by plasma-enhanced ALD and sputtering. Electrical characterization under ±0.9 V, 20 ns program/erase pulses reveal a memory window exceeding 1 V, a transient read-current ratio (I_{LVT}/I_{HVT}) greater than 10^4. Off-chip read measurements confirm a 50 ns read time with no observable latency in current sensing. Device-to-device variation analysis across 32 samples demonstrates robust switching uniformity and negligible performance scatter. Reliability benchmarks establish bipolar write endurance beyond 10^{12} cycles and read endurance exceeding 10^{12} cycles. Data retention tests at 85 °C show stable program and erase margins for over 10^4 s without refresh. To elucidate switching physics, a compact numerical model couples time-dependent Ginzburg–Landau equations for nucleation-limited ferroelectric dynamics with drift-diffusion transport in the IWO channel, calibrated via DC parameter extraction. Simulations capture percolation-driven steep-slope switching and predict intrinsic polarization reversal times down to ~1 ps, underscoring the feasibility of nanosecond-scale write operations. Performance benchmarking against state-of-the-art FEFETs highlights that the BEOL IWO FEFET achieves the highest endurance and largest memory window at the lowest operating voltage. The low thermal budget and amorphous oxide semiconductor channel facilitate seamless integration into standard CMOS back-end flows, enabling ultra dense, refresh-free last-level cache (LLC) and neuromorphic computing architectures. These results position BEOL-compatible IWO FEFETs as compelling candidates for next-generation embedded memory in advanced technology nodes, with future efforts focused on array-level integration, switching kinetics optimization, and three-dimensional system-on-chip deployment.

References

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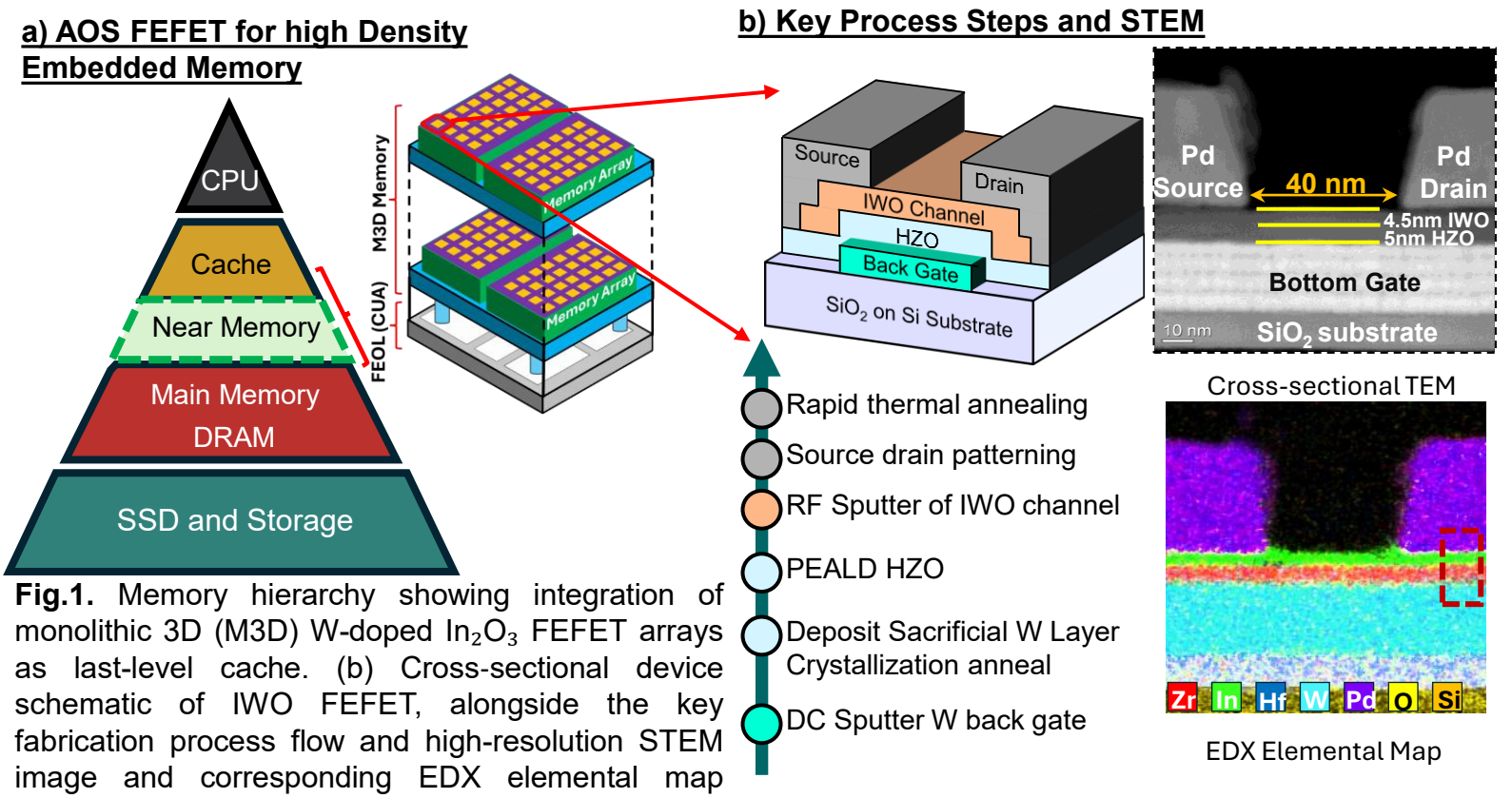

Fig.1. Memory hierarchy showing integration of monolithic 3D (M3D) W-doped In_2O_3 FEFET arrays as last-level cache. (b) Cross-sectional device schematic of IWO FEFET, alongside the key fabrication process flow and high-resolution STEM image and corresponding EDX elemental map confirming Zr, In, Hf, W, Pd, O and Si layer composition.

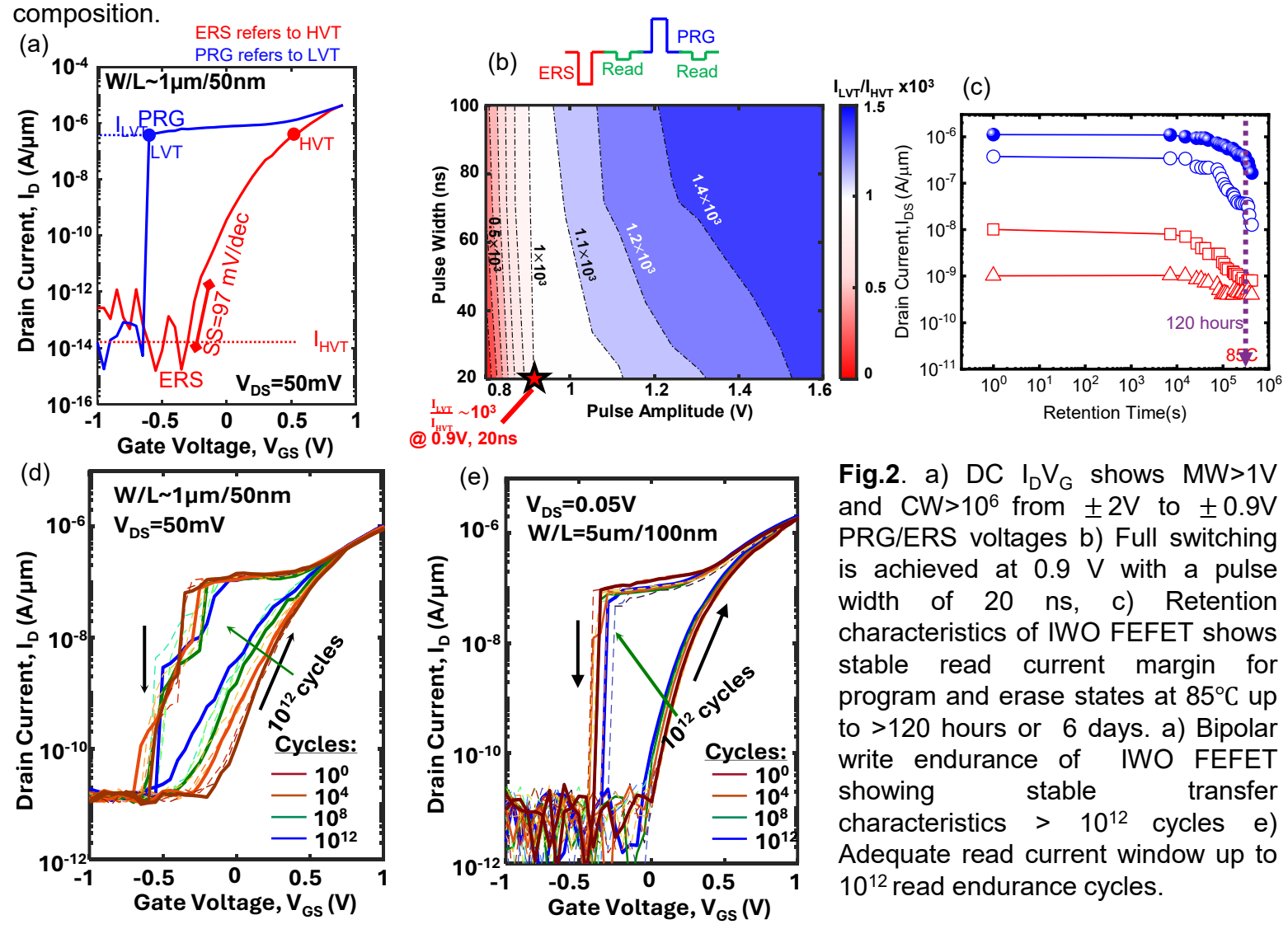

Fig.2. a) DC I_DV_G shows MW>1V and CW>10^6 from $\pm$2V to $\pm$0.9V PRG/ERS voltages b) Full switching is achieved at 0.9 V with a pulse width of 20 ns, c) Retention characteristics of IWO FEFET shows stable read current margin for program and erase states at 85℃ up to >120 hours or 6 days. a) Bipolar write endurance of IWO FEFET showing stable transfer characteristics > 10^{12} cycles e) Adequate read current window up to 10^{12} read endurance cycles.